OIPE IAP63
MAY 10 2006
PATENT & TRADEMARK OFFICE

FIG. 1 (PRIOR ART)

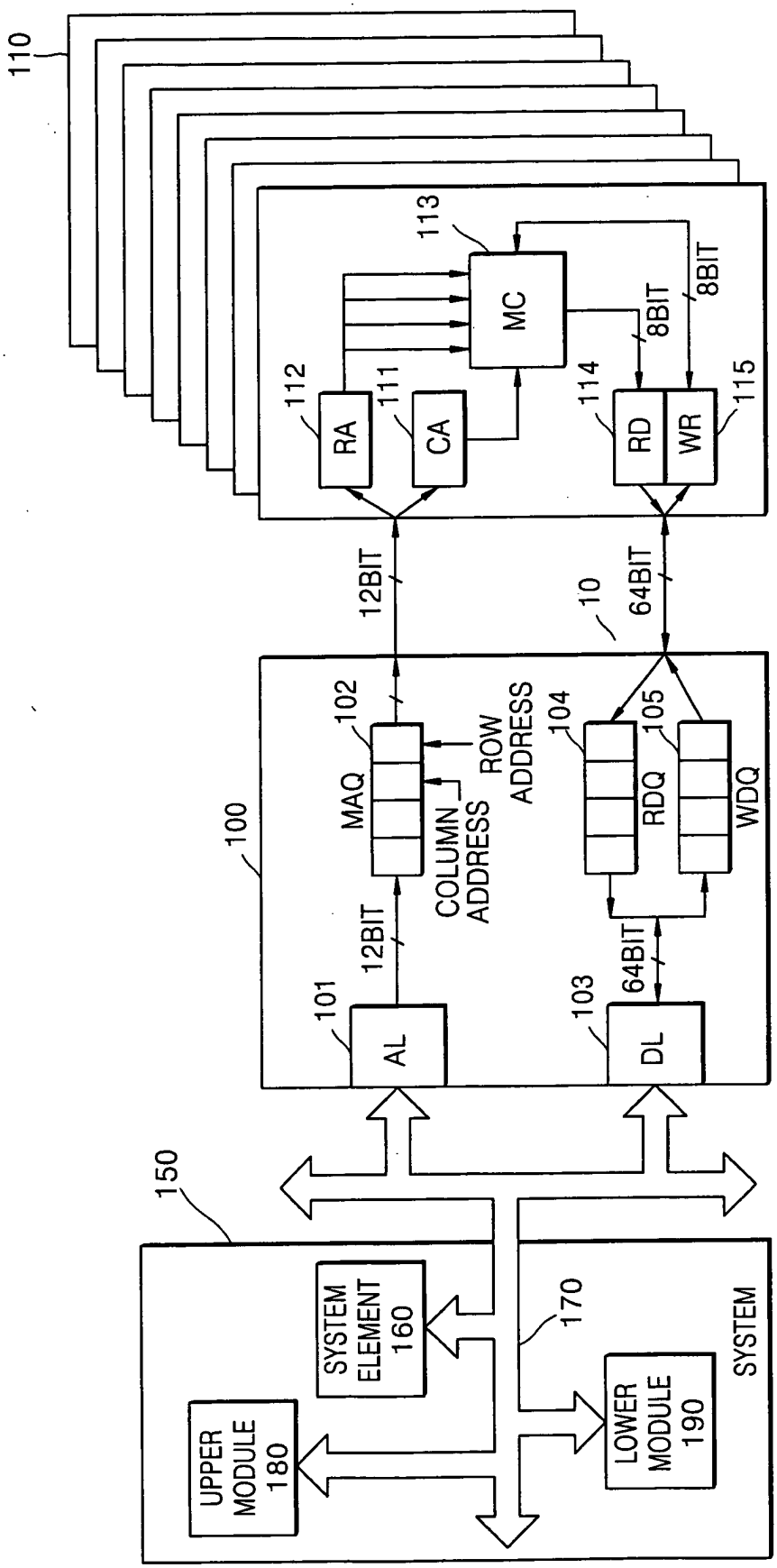


FIG. 3

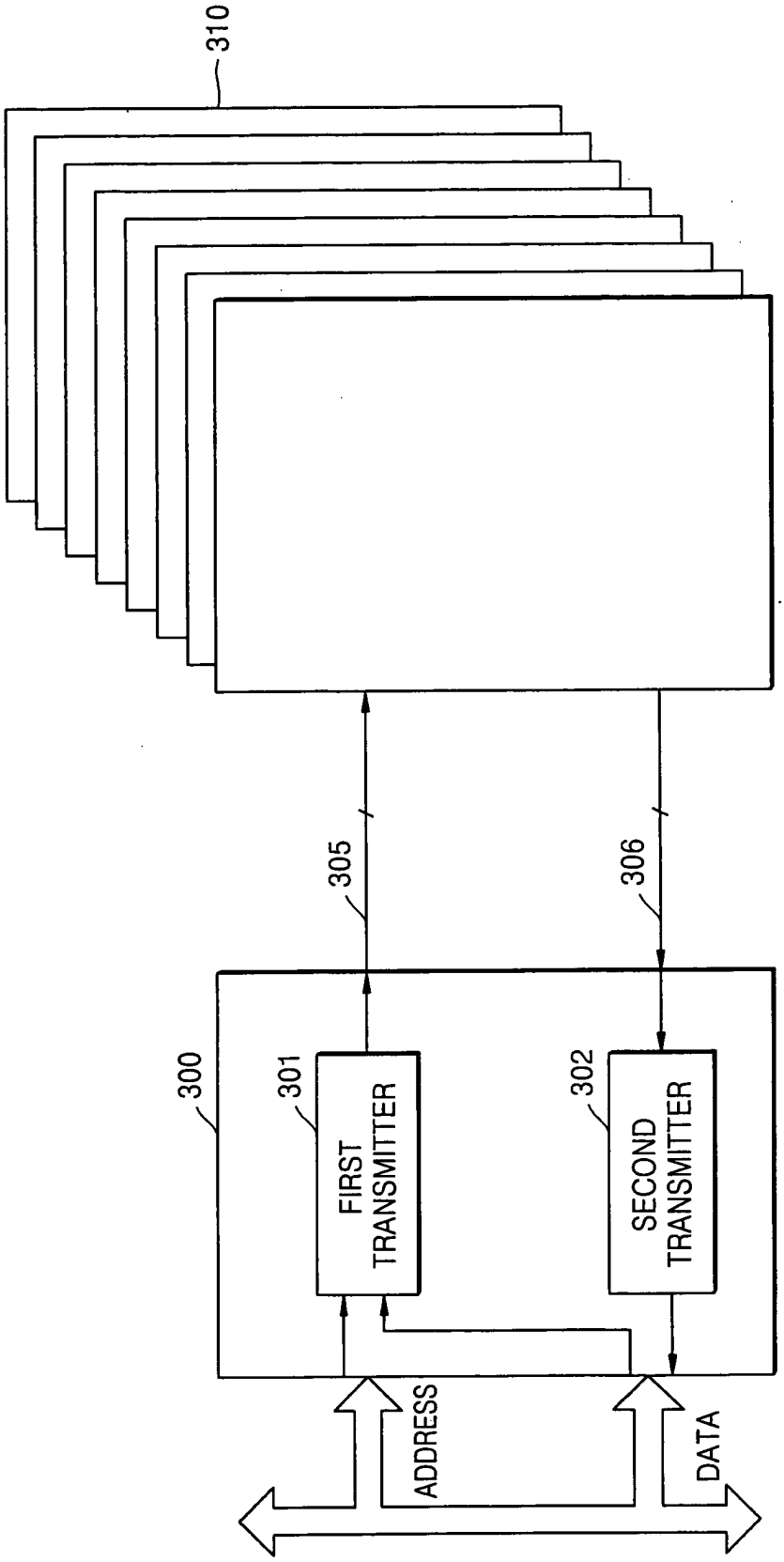
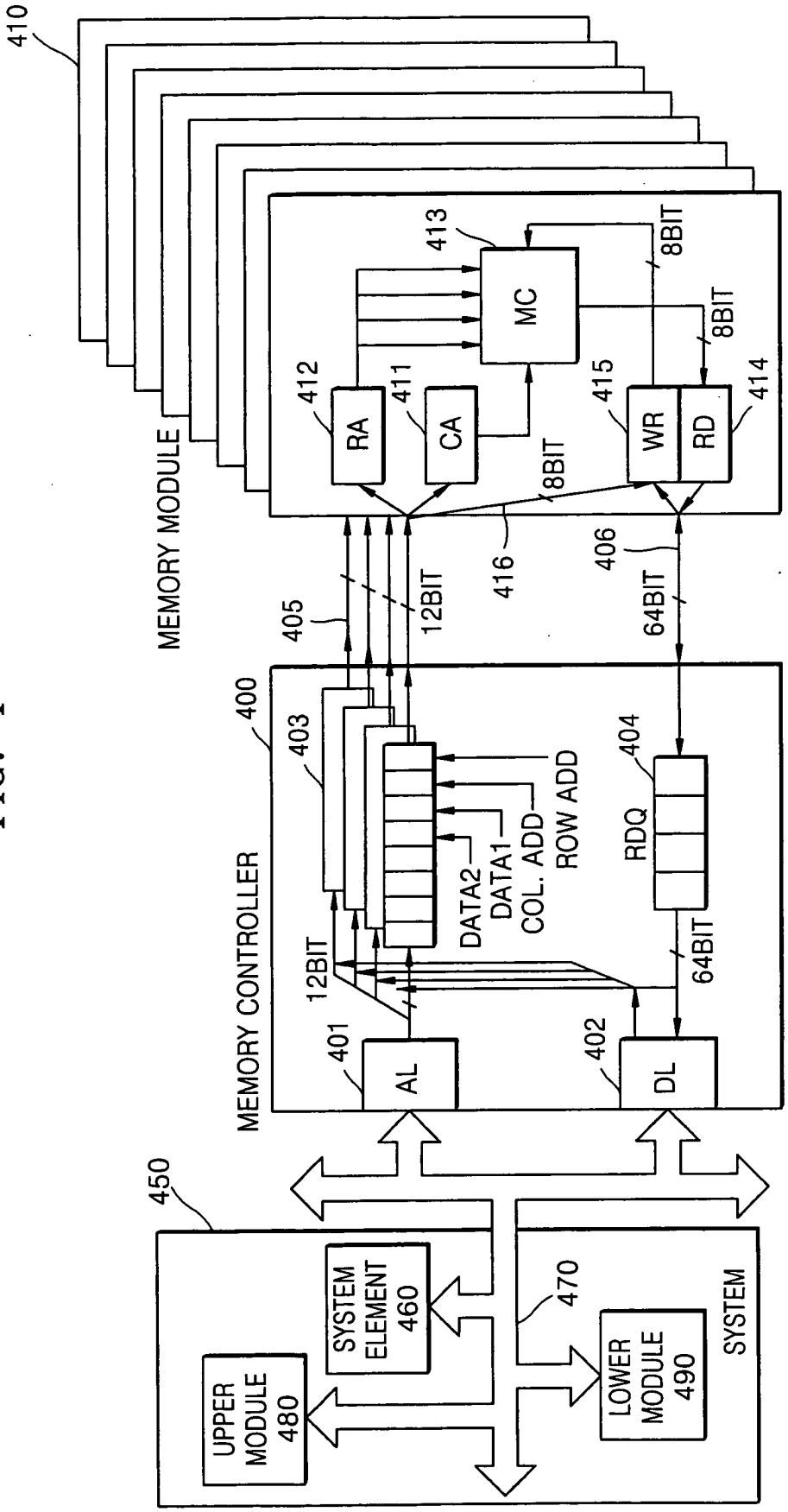

310
305
306
300
301
FIRST TRANSMITTER
302
SECOND TRANSMITTER
ADDRESS
DATA

FIG. 4


410
MEMORY MODULE
413
MC
8BIT
8BIT
412
RA
411
CA
415
WR
RD
414
8BIT
416
406
64BIT
405
12BIT
400
MEMORY CONTROLLER
403
404
RDQ
DATA2
DATA1
COL. ADD
ROW ADD
12BIT
64BIT
401
AL
402
DL
450
SYSTEM ELEMENT 460
UPPER MODULE 480
470
LOWER MODULE 490
SYSTEM

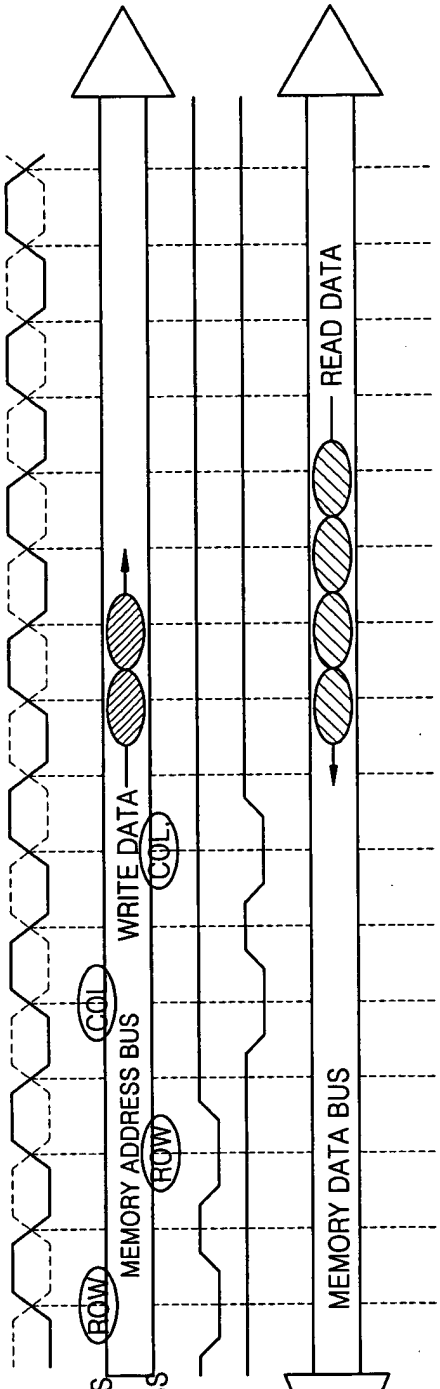


FIG. 5A
FIG. 5B
FIG. 5C
FIG. 5D
FIG. 5E

FIG. 6

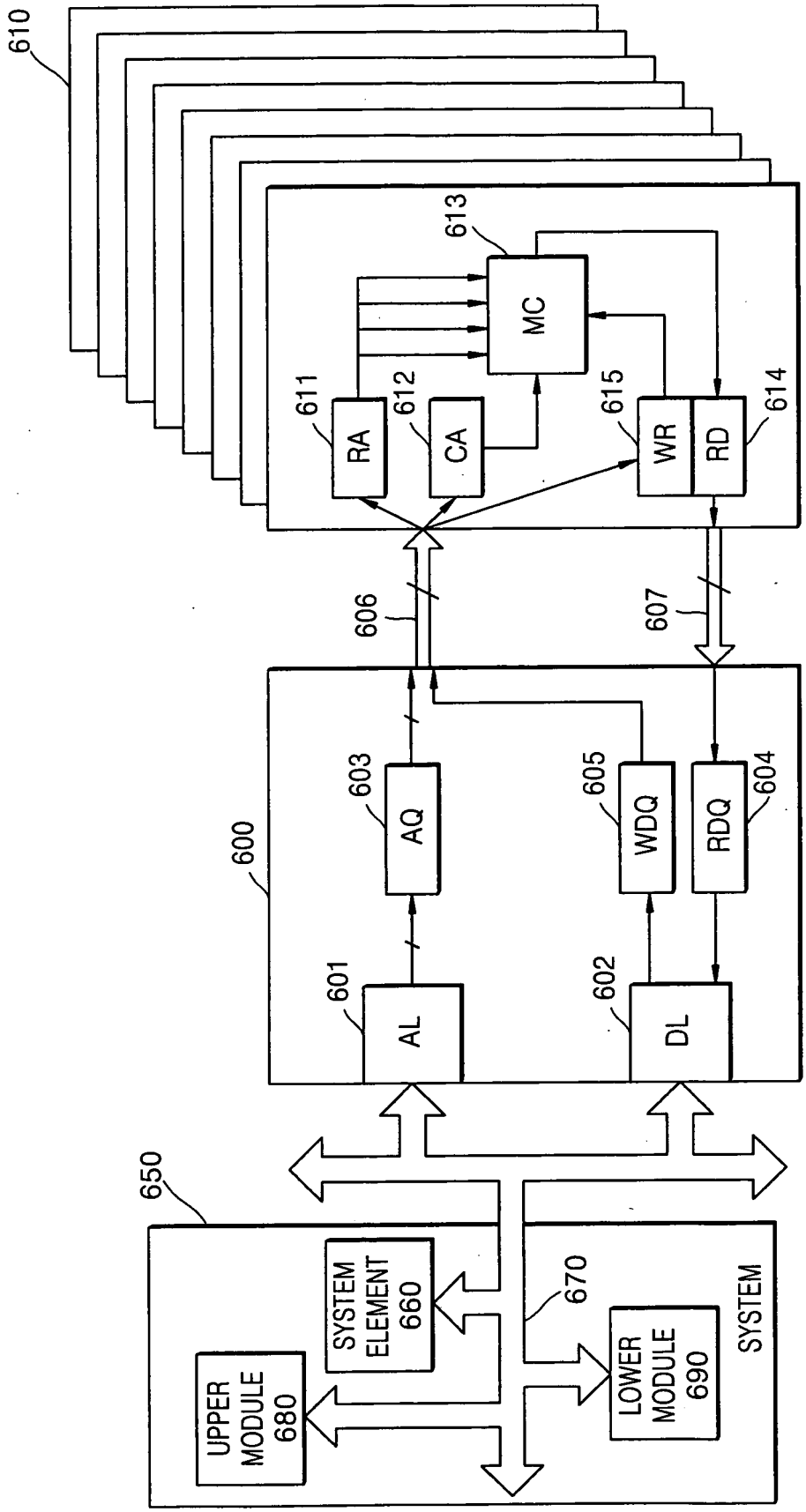
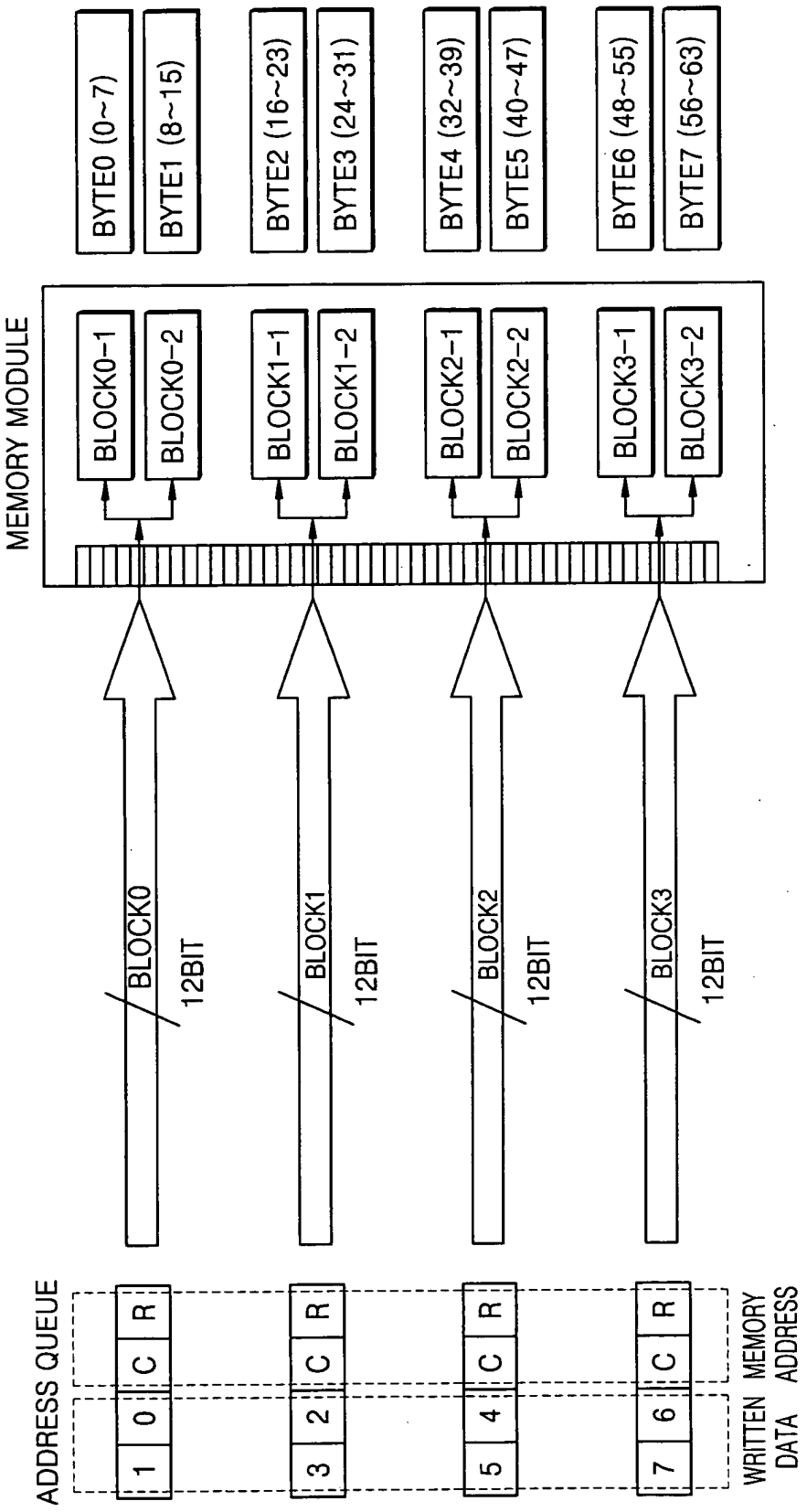

610
613
MC
611
RA
612
CA
615
WR
RD
614
606
607
600
603
AQ
605
WDQ
RDQ
604
601
AL
602
DL
650
SYSTEM ELEMENT 660
670
SYSTEM
UPPER MODULE 680
LOWER MODULE 690

FIG. 7


BYTE0 (0~7)
BYTE1 (8~15)
BYTE2 (16~23)
BYTE3 (24~31)
BYTE4 (32~39)
BYTE5 (40~47)
BYTE6 (48~55)
BYTE7 (56~63)
MEMORY MODULE
BLOCK0-1
BLOCK0-2
BLOCK1-1
BLOCK1-2
BLOCK2-1
BLOCK2-2
BLOCK3-1
BLOCK3-2
BLOCK0
12BIT
BLOCK1
12BIT
BLOCK2
12BIT
BLOCK3
12BIT
ADDRESS QUEUE
1
0
C
R
3
2
C
R
5
4
C
R
7
6
C
R
WRITTEN DATA
MEMORY ADDRESS